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Performance Analysis of MC-UPQC in Multi Feeder System

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Abstract: This paper aims to develop a Multi-converter unified power quality conditioner (MC-UPQC) and analyses performance with PI. Voltage and current disturbances, fluctuations and unbalance in multi feeder systems can be compensated simultaneously by using MC-UPQC system. Separating the series and the shunt compensation in the implementation this project carries out the MC-UPQC implementation. The shunt compensation is applied in the main feeder and the series compensation is carried out in the rest of the feeders connected in this multi feeder system. PI and d-q controller are used for the MC-UPQC implementation. In this paper, increases the power quality in multi feeders connected to two different power substations by using MC-UPQC. In this proposed topology all the voltage source converters are connected to common DC link capacitor. Implementation is done by MATLAB and the results are obtained.

Keywords: Unified Power quality conditioner (UPQC), Multi-converter unified power quality conditioner (MC-UPQC), Power quality (PQ), Voltage source converter (VSE).

I. INTRODUCTION

This For proper functioning of electronic devices voltage flowing should be within a consistent range. Power surges, sags/swells disturbances and momentary interruption will cause voltage to vary outside the consistent range. Due to increasing usage of nonlinear and electronic switching equipments in distribution system PQ problems will occurs. Along with these, lightening hit on transmission line, capacitor bank, improper wiring can also cause PQ problems. Some loads that can gradually degrade internal circuitry of sensitive equipments.

It is necessary to reach PQ rated limits by using few sort to counterbalance the load and source parameters like voltages and current. The modern solution found to compensate is usage of active power filters (APF). According to a system configuration APF is classified as series-APF and shunt-APF. The series-APF compensates the distortions in the voltage, same way distortions in the current are compensated by shunt APF. The series-APF and shunt-APF together forms the UPQC.

Voltage Source Converter (VSC)- power devices are extensively used in PQ refinement in distribution system. In the different types of VSC devices, one is Distribution Static.Compensator (DSTATCOM) which can be used to compensate variation and unbalance in a load and made to flow a compensated balanced current through the feeder [3]. This can also synchronize the distribution bus voltage[3]. Another one is Dynamic0Voltage Restorer (DVR) [4] which is used to compensate voltage distortions and imbalance in supply voltage and it can be used to regulate voltage in a critical load terminals [5], [6].
FACTS devices are used to compensate the disturbances present in multi lines. Main function of these two devices is to control, current and voltage distortions of multi line or sub network instead of single line power flow control.

The FACTS devices classified based on their converter used in system. One is Interline Power Flow Controller(IPFC), it consist of two series VSCs(Se-VSC) with the common dc link capacitor. If the power flows through inter lines initiating from same substation is controlled by this device. It allows to circulate active power in between the Se-VSCs. Along with this compensation, to optimize network utilization two inter lines to be controlled simultaneously [7].

Another FACTS device is Generalized-Unified Power Flow Controller (GUPFC) [8]. This is one of the method for compensation in which three VSC controller are used out of which one is shunt-VSC(Sh-VSC) and other two are Se-VSC which are connected to DC-link capacitor. GUPFC is capable of controlling five quantities of power system they are real power and reactive power present in two parallel inter lines along with sending end bus voltage simultaneously[8].

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The new topology of UPQC is multi converter-UPQC is explained in [1]. The proposed method consist of two Se-VSCs which are connected in series with the multi feeders and one Sh-VSC connected in parallel with the main feeder as that in GUPFC but the difference is that the two feeders not supplied by the same substation. The Result obtained in MATLB in two feeders system show the result configuration of new topology.

II. STRUCTURE OF MC-UPQC

A. Circuit Diagram

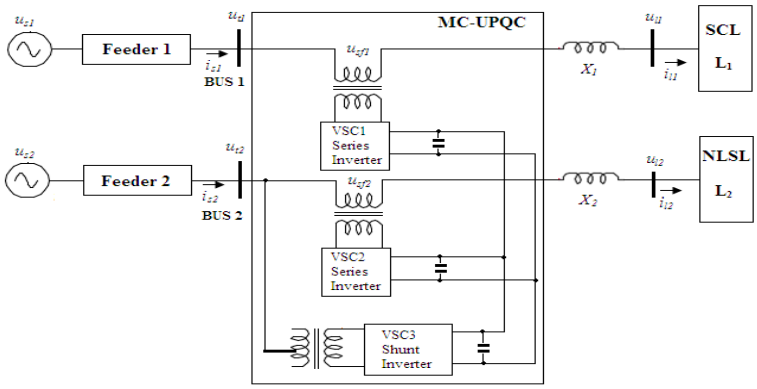

Figure 1: Schematic diagram of proposed MC-UPQC

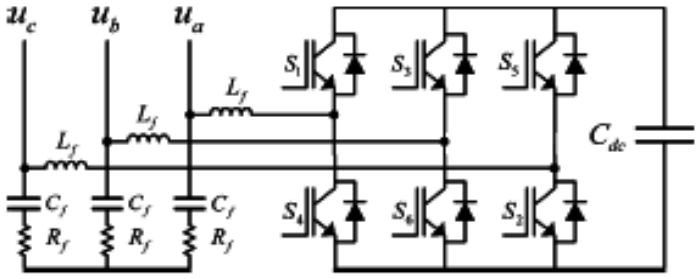

Figure:2 Typical VSC controller structure

The schematic diagram of MC-UPQC system which has two parallel feeders supplied by two separate substations with the different load L_1 and L_2 is as shown in figure1. The load L_1 is considered as sensitive/critical load (SCL) this consist of non-sinusoidal voltage, sag/swell and interruptions. The load L_2 is considered as the nonlinear/sensitive load (NLSL) consist of non-sinusoidal current and distorted voltage also contains harmonics. These load have to be protected against distortions, interruptions and harmonics to improve PQ.

BUS1 and BUS2 are the two different buses connected to MC-UPQC system with the bus voltages of u_{t1} and u_{t2} respectively. The feeder currents are represented by i_{s1} and i_{s2}. Shunt VSC and series VSC are a part of MC-UPQC. u_{s1} and $\mathbf{u_{s2}}$ are supply voltage. u_{l1} and u_{l2} are load voltages. Bus voltages are u_{t1} and u_{t2} which are unbalanced and put into sag or swell.

Typical VSC controller structure is as shown fig.2. The VSC is consist of filters like commutation reactor(L_f) and high pass output filter ($R_f C_f$). These filters are used to decrease the switching harmonics flowing towards power supply.

The main functions of the MC-UPQC system are:

1) To protect the load voltages like u_{l2} and u_{l2} against interruptions, fluctuation, imbalance and power surges.
2) Reactive power and harmonic present in nonlinear load current (i_{l2}) are compensated by proposed system.

B. Control Strategy

Multi converter-UPQC system consist of one shunt-VSC, two series-VSCs those are connected to common DC-link capacitor and are can be control independently. Series-VSC with the Sinusoidal Pulse Width Modulation(SPWM) switching strategy is used for voltage compensation. Same way shunt-VSC with the hysteresis switching strategy is used for current control. The control algorithm used here is d-q control method.

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I. Shunt VSC

Function of shunt VSC:

1) To compensate harmonic distortions and reactive components present in nonlinear load current (i_{l2});
2) To regulate the dc link capacitor voltage.

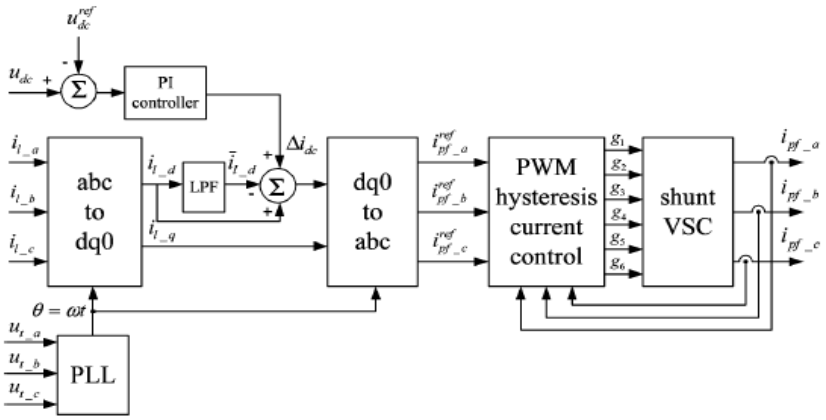

Figure.3. shunt VSC control structure

Shunt VSC control structure is shown in figure.3. By using park transformation method load current($i_{l_{dq0}}$) is obtained. The obtained load current ($i_{l_{dq0}}$) is given in equation 1

$$i_{l_{dq0}} = T_{abc}^{dq0}\, i_{l_{abc}} \quad \text{.....(1)}$$

where the transformation matrix is given by

$$T_{abc}^{dq0} = 2/3 \begin{bmatrix} cos(wt) & cos(wt-120) & cos(wt+120) \\ -sin(wt) & -sin(wt-120) & -sin(wt+120) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \text{.....(2)}$$

Usage of Low Pass Filter(LPF) helps to obtain the fundamental positive sequence component for DC quantities in d and q axis by using transformation equation. And also AC quantities are obtained by fundamental frequency shift of all the harmonic components.

$$i_{l\_d} = \bar{\imath}_{l\_d} + \tilde{\imath}_{l\_d} \quad \text{.....(3)}$$
$$i_{l\_q} = \bar{\imath}_{l\_q} + \tilde{\imath}_{l\_q} \quad \text{.....(4)}$$

Where i_{l_d} and i_{l_q} are in load current with d-q components. $\bar{\imath}_{l\_d}$, $\bar{\imath}_{l\_q}$ are the fundamental positive sequence component with the dc components in d and q axis are obtained by using transformation equation. $\tilde{\imath}_{l\_d}$, $\tilde{\imath}_{l\_q}$ are the ac quantities obtained by fundamental frequency shift of all the harmonic components.

The d-q components of Sh-VSC current are given by below equations

$$i_{pf\_d}^{ref} = \bar{\imath}_{l\_d} \quad \text{.....(6)}$$
$$i_{pf\_q}^{ref} = i_{l\_q} \quad \text{.....(7)}$$

Similarly, feeder currents i_{s2} in d-q component are given by

$$i_{s\_d} = \bar{\imath}_{l\_d} \quad \text{.....(7)}$$
$$i_{s\_q} = 0 \quad \text{.....(8)}$$

Above equations shows that feeder current i_{s2} is free from switching losses and reactive components. These losess and other disturbances like sudden variation of non-leniar load current cause to decrase the voltage of DC-link capacitor. To control DC-link capacitor voltage PI controller is used. Input for the PI controller is differenc between the actual capacitor voltage (u_{dc}) and its reference voltage (u_{dc}^{ref}) is given as. Summation of PI controller output and the shunt VSC reference current of d component will give a new reference current. The new reference currents given by

$$\begin{cases} i_{pf\_d}^{ref} = \bar{\imath}_{l\_d} + \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \quad \text{.....(9)}$$

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Reference shunt VSC current in equation 9 is transformed back to abc reference frame by using inverse perk transformation method and is given by equation 10 .

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc}\, i_{pf\_dq0}^{ref}; \left(T_{dq0}^{abc} = T_{abc}^{dq0^{-1}}\right) \text{ ……..(10)}$$

The output compensting current in each phase are obtained by PWM hysteresis current control method

II. Series VSC

Functions of series VSC are:

1) Used to reduce voltage surges;
2) Used to compensate harmonics present in voltage distortions;
3) Used to compensate interruptions present in feered 1 only.

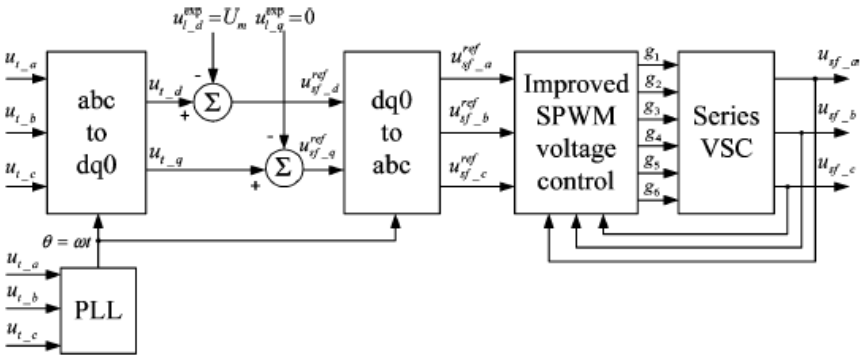

Figure.4. control structure of series APF

Figure 4. shows the control structure of Se-VSC. The bus voltage (u_{t_abc}) is found by using park transformation method. Bus voltage (u_{t_abc})

$$u_{t\_dq0} = T_{abc}^{dq0} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \text{ ..(11)}$$

where

$$\begin{cases} u_{t1p} = [u_{tlpd} \quad u_{t1pq} \quad 0]^T \\ u_{t1n} = [u_{t1n\_d} \quad u_{t1n\_q} \quad 0]^T \\ u_{t10} = [0 \quad 0 \quad u_{00}]^T \\ u_{th} = [u_{th\_d} \quad u_{th\_q} \quad u_{th\_0}]^T \end{cases} \text{ ……..(12)}$$

The +ve, -ve and zero sequence frequency components represented by u_{t1p}, u_{t1n} and u_{t10}. Harmonic component present in bus voltage is represented by u_{th}.

According to MC-UPQC control objectives, even though the bus voltages u_{t1} and u_{t2} are varied the load voltages u_{l1} and u_{l2} must kept in sinusoidal with constant magnitude like amplitude. Therefore, the required load voltage $u_{l\_dq0}^{ref}$ only has one value, and is obtained by the synchronous dq0 reference frame

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0} u_{l\,abc}^{exp} = \begin{bmatrix} u_m \\ 0 \\ 0 \end{bmatrix} \text{ ……(13)}$$

In the above equation expected load voltage $u_{l\_abc}^{exp}$ is given by

$$u_{l\_abc}^{exp} = \begin{bmatrix} u_m \cos(wt) \\ u_m \cos(wt - 120) \\ u_m \cos(wt + 120) \end{bmatrix} \text{ ……(14)}$$

Compensating reference voltage $u_{sf\_dq0}^{ref}$ in the synchronous dq0 reference frame is defined as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \text{ ……..(15)}$$

The reference voltages after compensation are given in equation 15, is transformed back to the abc reference frame by using inverse park transformation method.

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III. SIMULATION RESULTS

The performance.of MC-UPQC has been tested by considering different type of controller using MATLAB simulation. In this section, simulation result is presented and performance of the system by using PI controller is verified.

Table 1: Load Specifications

Type of Load	**Specifications**
Nonlinear/sensitive Load(NLSL), L_1	3 phase rectifier load R= 1Ω and L=10mH
Sensitive/critical Load(SCL), L_2	R= 40Ω and L=10mH

Let us assume that MC_UPQC power system in fig.1 contains two 3 phase-3 wire 250V (rms, L-L), 50Hz practicabilities. The BUS1.voltage (u_{t1}) consist of 35% of fifth order harmonics and 35% sag between the value of $0.15s < t < 0.25s$. The BUS2 voltage (u_{t2}) contains 22% of seventh order harmonics and 22% of sag between the value of $0.1s < t < 0.25s$.

Table 2: Simulation Parameters

Notifications	**Specifications**
Supply Voltage(V_s)	250V Line-Line
Commutation Reactor (L_f)	800μH
High pass output filter (R_f , C_f)	Rf=8Ω Cf=50μF
DC bus voltage(V_{dc})	500V

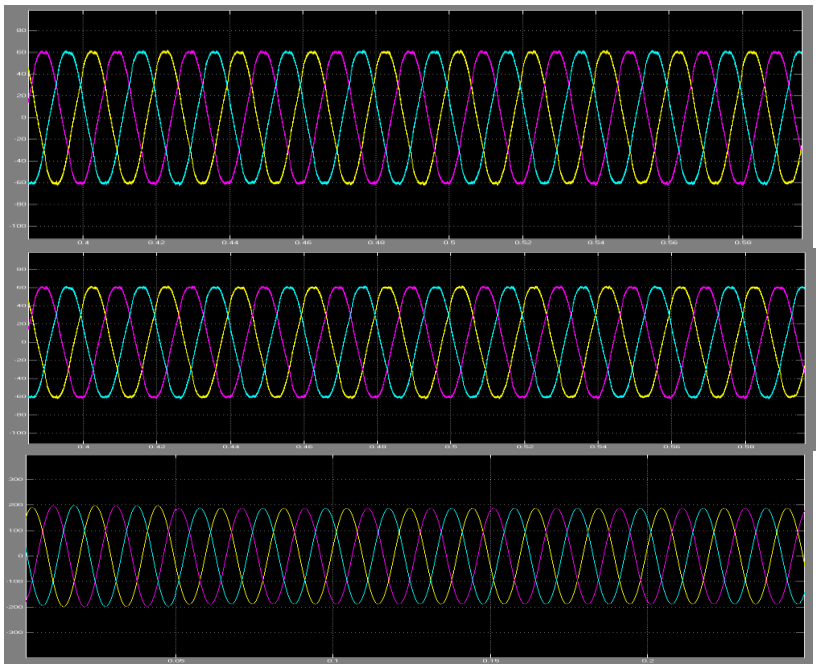
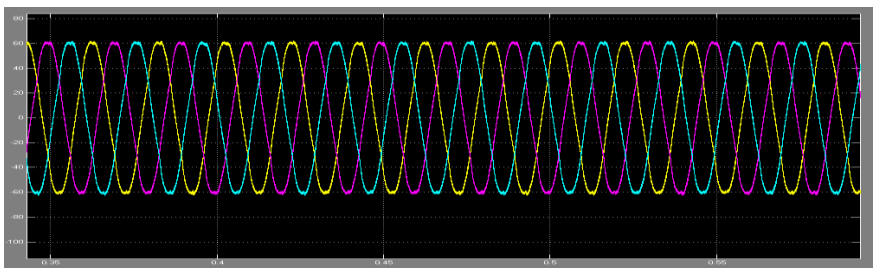


Figure:5. Sensitive critical load (L_2) voltage, BUS1 voltage before compensation and BUS1 voltage after compensation.



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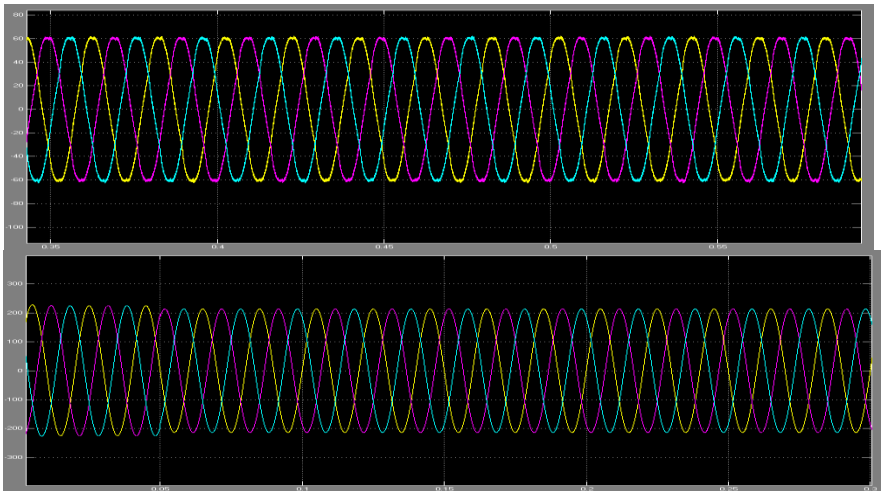

Figure:6. Nonlinear load (L_1) voltage, BUS2 voltage before compensation, and BUS2 voltage after compensation.

MC-UPQC power system is switched ON at switching time t=0.02s. Sensitive/critical Load. voltage, BUS1.voltage u_{t1} before compensation and after compensation are shown in fig7. Similarly, Figure8 shows that the nonlinear load voltage, BUS2 voltage u_{t2} before compensation and after compensation. These figures explains that the distorted voltages of BUS1 and BUS2 are compensated satisfactorily with the very good dynamic response of load L_1 and L_2 .

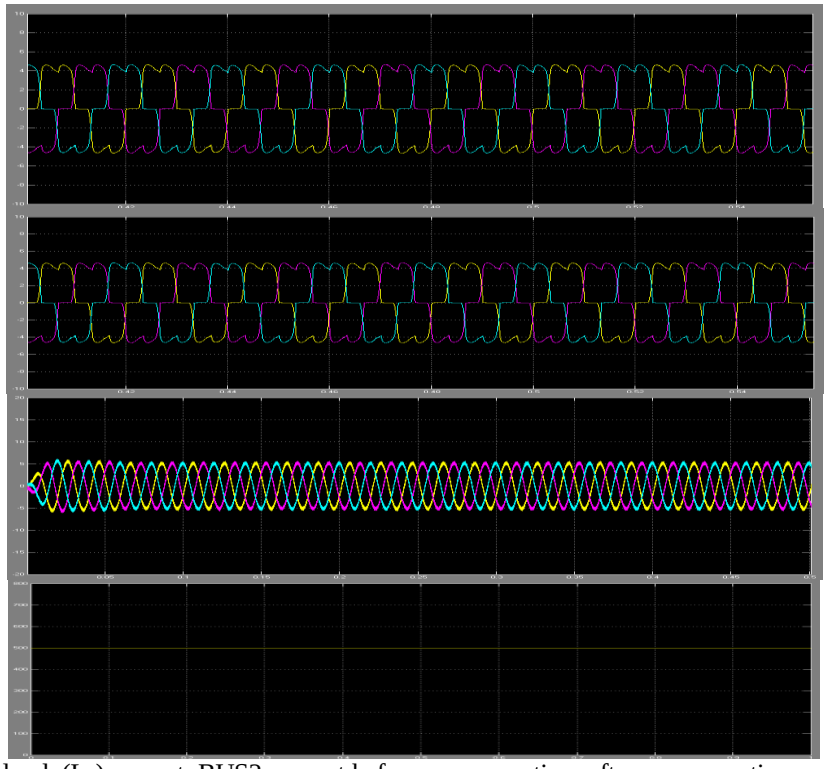

Figure:7. Nonlinear load (L_1) current, BUS2 current before compensation, after compensation and DC link capacitor voltage

The nonlinear/sensitive load current i_{l2}, BUS2 current before compensation, after compensation and voltage of DC-link capacitor are shown in figure.7.

The DC-link capacitor serves 2 purposes

1) It maintains nearly a continuing DC voltage
2) It is associate in nursing energy storage component to produce real power distance between load and supply throughout transients.

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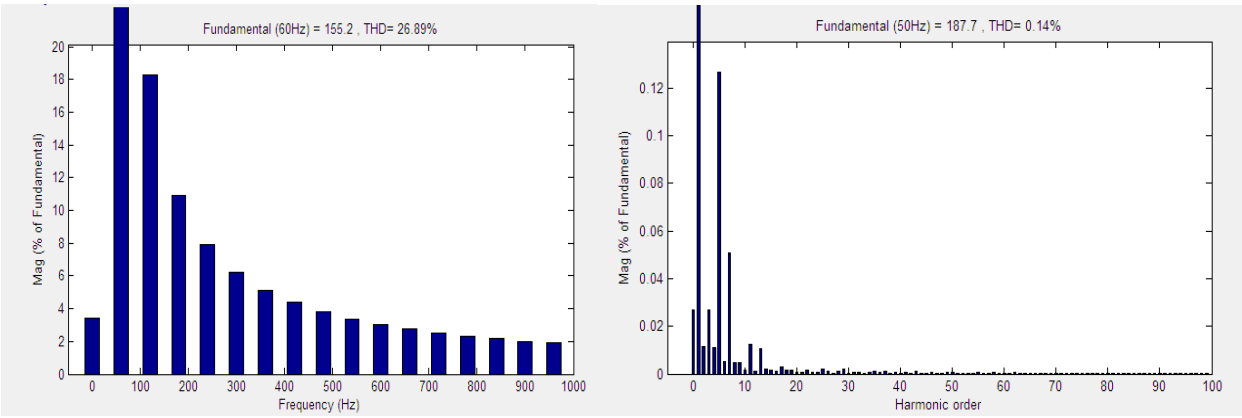

Figure:8. THD of BUS1 voltage before compensation and after compensation

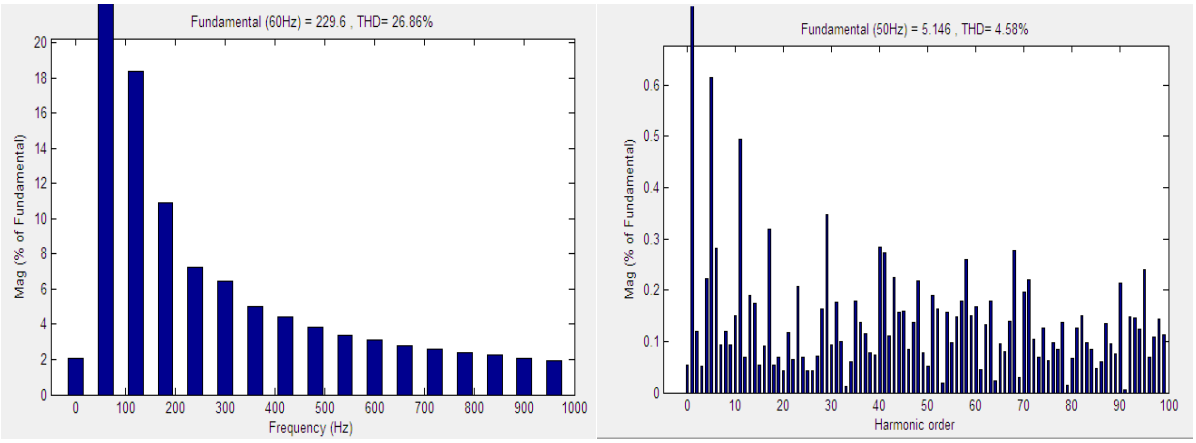

Figure:9. THD of BUS2 current before compensation and after compensation.

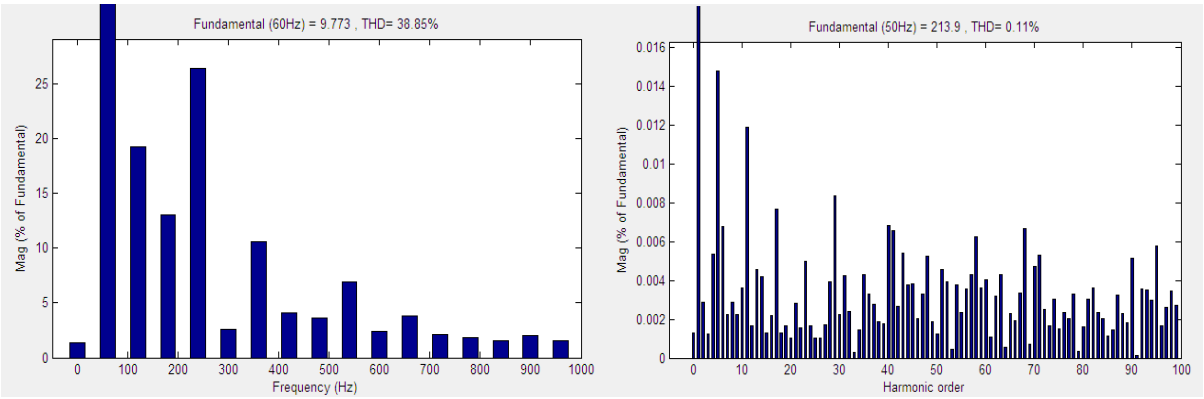

Figure:10. THD of BUS2 voltage before compensation and after compensation.

Total Harmonic-Distortion (THD) of the feeder current and voltages should be maintained in between 0 to 5% for proper functioning of the system. The.THD of BUS1 voltage is decreased from 26.89% to 0.14% and that of BUS2 voltage is decreased from 38.85% to 0.11% and for current is reduced from 26.86% to 4.58%. These THD configuration are shown in figure:8,9 and 10. The simulation results obtained by proposed MC-UPQC with PI controller are shown in figures:5, 6 and 7.

IV. CONCLUSION

The paper explains that MC-UPQC system is used to compensate harmonics present in two different feeders starting from different substations The three voltage source converters are used one is Sh-VSC and two Se-VSCs share a common dc link capacitor. The controller used here is PI. This topology shows that MC-UPQC can control

simultaneously voltage and current distortions, sag/swell and removes the harmonics in different feeders coming from different substations compares the variation in THD of the system before compensation and after compensation. The results obtained by using MATLAB simulation circuit.

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BIOGRAPHIES

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